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Title: PARALLEL EQUALIZATION FOR SYSTEMS USING TIME DIVISION MULTIPLE ACCESS

Amendment to the Drawings

The attached sheet(s) of drawings include changes to Fig(s). 3 & 4. These sheet(s), which include Fig(s).3 & 4, replaces the original sheet(s) including Fig(s). 3 & 4. Figure 3 has been amended to show control signal 314 in equalizer 304 which goes to selector circuit 310. Figure 4 has been amended to show decoder bank 412 within equalizer circuit 400.

Attachments: Replacement sheet(s)

Annotated sheet(s) showing changes

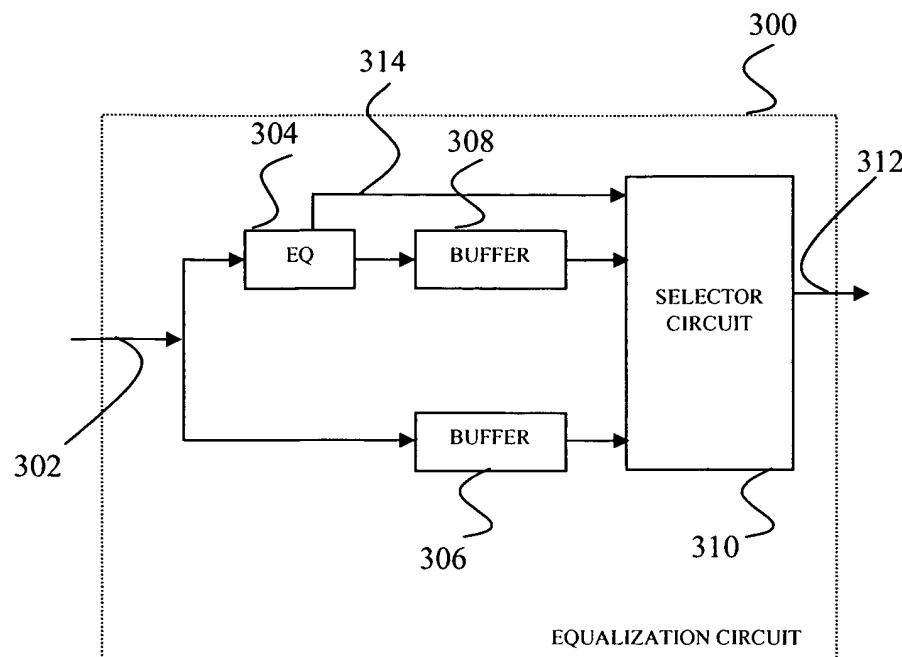


FIG. 3

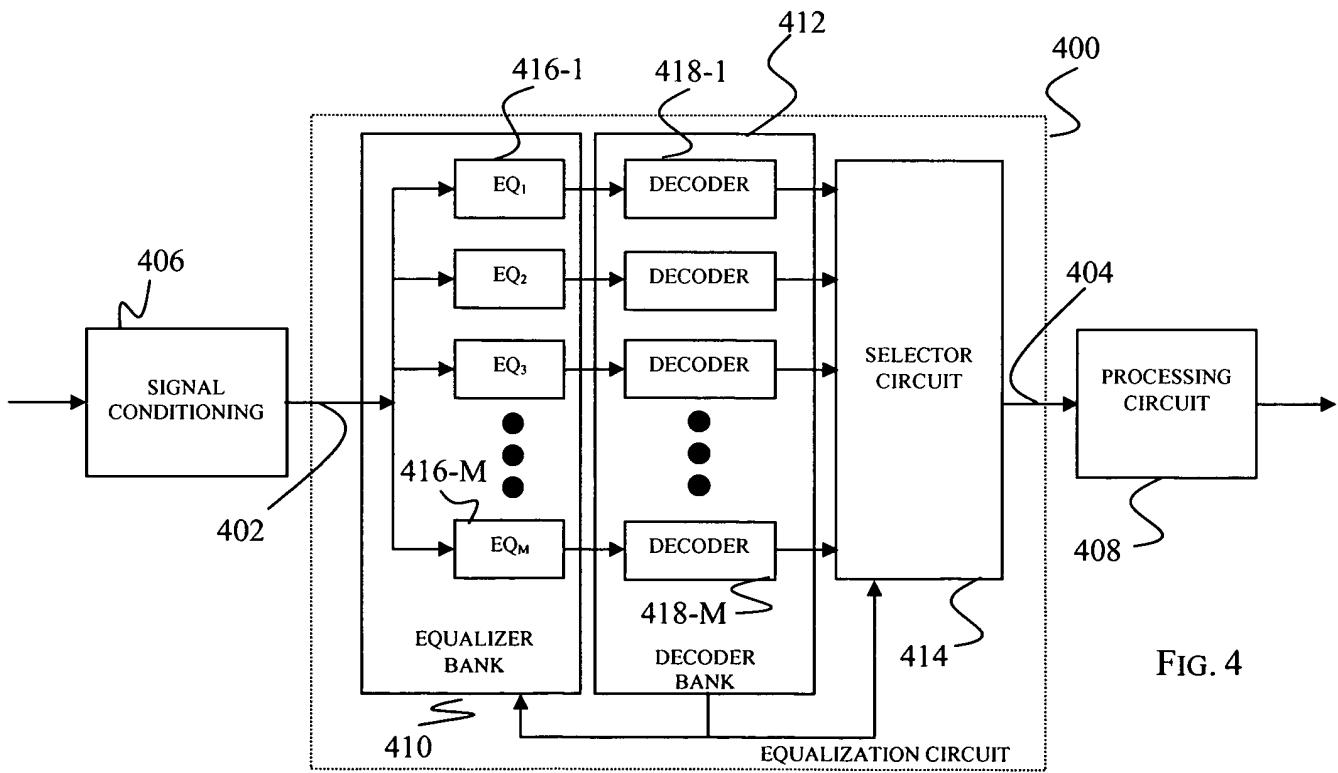


FIG. 4